Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of designing a test structure, comprising:
defining and placing test circuit pins in an integrated circuit design;
routing one or more fat wires, each fat wire routed between a set of said test circuit pins;
processing each fat wire into a continuous wire and one or more corresponding wire segments adjacent to said continuous wire, said continuous wire separated from said one or more corresponding wire segments by a space; and
connecting said continuous wire and said one or more wire segments to circuit elements of a defect monitor scan chain, said circuit elements previously inserted into said integrated circuit design.

[c2] 2. The method of claim 1, wherein said test circuit pins include pins of said previously inserted circuit elements.

[c3] 3. The method of claim 1, wherein said test circuit pins include proxy pins placed away from and corresponding to one or more pins of said previously inserted circuit elements.

[c4] 4. The method of claim 1, further including, when more than one fat wire has been routed, routing additional wires to electrically connect each continuous wire in series.

[c5] 5. The method of claim 4, wherein two or more fat wires have different widths.

[c6] 6. The method of claim 1, further including, when more than one fat wire has been routed, routing at least a first fat wire of said one or more fat wires in a first circuit block of said integrated circuit design and routing at least a second fat wire of said one or more fat wires in a second circuit block of said integrated circuit design.

[c7] 7. The method of claim 1, when more than one fat wire has been routed, routing at least a first fat wire of said one or more fat wires in a first wiring level of said integrated circuit design and routing at least a second fat wire of said one or more fat wires in a second wiring level of said integrated circuit design.

[c8] 8. The method of claim 1, further including:

placing at least one intermediate point in said integrated circuit design; and

said routing of one or more fat wires between sets of two or more of said test circuit pins includes routing

at least one of said fat wires to said at least one intermediate point.

[c9] 9. The method of claim 1, further including:
connecting said defect monitor scan chain to a functional and parametric test scan chain previously inserted into said integrated circuit design.

[c10] 10. The method of claim 1, wherein said defect scan chain includes a first set of latches, a second set of latches and gates and the method further including:
routing first wires between said first set of latches and said continuous wire at locations along the length of said continuous wire located between wire segments;
routing second wires between said second set of latches and corresponding conductor segments of multiplicity of conductor segments; and
routing third wires to connect said gates between ends of pairs of said wire segments.

[c11] 11. A computer system comprising a processor, an address/data bus coupled to said processor, and a computer-readable memory unit coupled to said processor, said memory unit containing instructions that when executed by said processor implement a method for designing a test structure, said method comprising the computer implemented steps of:

placing test circuit pins in an integrated circuit design;
routing one or more fat wires, each fat wire routed between a set of said test circuit pins;
processing each fat wire into a continuous wire and one or more corresponding wire segments adjacent to said continuous wire, said continuous wire separated from said one or more corresponding wire segments by a space; and
connecting said continuous wire and said one or more wire segments to circuit elements of a defect monitor scan chain, said circuit elements previously inserted into said integrated circuit design.

[c12] 12. The system of claim 11, wherein said test circuit pins include pins of said previously inserted circuit elements.

[c13] 13. The system of claim 11, wherein said test circuit pins include proxy pins placed away from and corresponding to one or more pins of said previously inserted circuit elements.

[c14] 14. The system of claim 11, the method further including, when more than one fat wire has been routed, routing additional wires to electrically connect each continuous wire in series.

[c15] 15. The system of claim 14, wherein two or more fat

wires have different widths.

[c16] 16. The system of claim 11, further including, when more than one fat wire has been routed, routing at least a first fat wire of said one or more fat wires in a first circuit block of said integrated circuit design and routing at least a second fat wire of said one or more fat wires in a second circuit block of said integrated circuit design.

[c17] 17. The system of claim 11, when more than one fat wire has been routed, routing at least a first fat wire of said one or more fat wires in a first wiring level of said integrated circuit design and routing at least a second fat wire of said one or more fat wires in a second wiring level of said integrated circuit design.

[c18] 18. The system of claim 11, the method further including:

placing at least one intermediate point in said integrated circuit design; and

said routing of one or more fat wires between sets of two or more of said test circuit pins includes routing at least one of said fat wires to said at least one intermediate point.

[c19] 19. The system of claim 11, the method further including:

connecting said defect monitor scan chain to a functional and parametric test scan chain previously inserted into said integrated circuit design.

[c20] 20. The system of claim 11, wherein said defect scan chain includes a first set of latches, a second set of latches and gates and the method further including:

routing first wires between said first set of latches and said continuous wire at locations along the length of said continuous wire located between wire segments;

routing second wires between said second set of latches and corresponding conductor segments of multiplicity of conductor segments; and

routing third wires to connect said gates between ends of pairs of said wire segments.